WHAT IS CLAIMED IS:

1. A calibration circuit, comprising:

first and second digitally tunable filters; and

control logic to digitally tune the first and second filters as a function of a first parameter of a first signal output from the first filter and a second parameter of a second signal output from the second filter.

2. The calibration circuit of claim 1 wherein the first and second filters each comprises a polyphase filter.

3. The calibration circuit of claim 1 wherein the first and second filters each comprises a notch filter.

4. The calibration circuit of claim 1 further comprising a first signal strength indicator to determine the first parameter and a second signal strength indicator to determine the second parameter.

5. The calibration circuit of claim 4 wherein the first parameter comprises a first signal suppression and the second parameter comprises a second signal suppression.

6. The calibration circuit of claim 5 further comprising a comparator to compare the first signal suppression to the second signal suppression, the control logic digitally tuning the first filter if the first signal suppression is lower than the second signal suppression and digitally tuning the second filter if the second signal suppression is lower than the first signal suppression.

7. The calibration circuit of claim 6 wherein the control logic digitally tunes each of the first and second filters by providing a first digital word to the first filter and a second digital word to the second filter.

8. The calibration circuit of claim 1 wherein the first filter comprises a first resistor and first tunable capacitor, and the second filter comprises a second resistor and a second tunable capacitor, the control logic digitally tuning the first and second capacitors.

9. The calibration circuit of claim 8 wherein the control logic digitally tunes each of the first and second capacitors by providing a first digital word to the first capacitor and a second digital word to the second capacitor.

10. The calibration circuit of claim 9 wherein the control logic tunes initially tunes the first capacitor to a first value and tunes the second capacitor to a second value different from the first value, and wherein the control logic is disabled when the first digital word equals the second digital word.

11. The calibration circuit of claim 10 wherein the first value comprises a maximum value of the first capacitor and the second value comprises a minimum value of the second capacitor.

12. The calibration circuit of claim 8 wherein the first capacitor comprises a first tunable capacitor array and the second capacitor comprises a second tunable capacitor array.

13. The calibration circuit of claim 12 wherein the first and second tunable capacitor arrays each comprises a plurality of capacitors coupled in parallel, and a plurality of switches each being coupled in series to a different one of their its respective capacitors.

14. The calibration circuit of claim 13 wherein the control logic tunes the first filter with a plurality of first digital bits and tunes the second filter with a plurality of second digital bits, the first digital bits each controlling a different one of the switches in the first capacitor array and the second digital bits each controlling a different one of the switches in the second capacitor array.

15. A calibration circuit, comprising:

first and second digitally tunable filters; and

tuning means for digitally tuning the first and second filters as a function of a first parameter of a first signal output from the first filter and a second parameter of a second signal output from the second filter.

16. The calibration circuit of claim 15 wherein the first and second filters each comprises a polyphase filter.

17. The calibration circuit of claim 15 wherein the first and second filters each comprises a notch filter.

18. The calibration circuit of claim 15 wherein the first parameter comprises a first signal suppression and the second parameter comprises a second signal suppression, the tuning means further comprising means for determining the first signal strength of the first signal output from the first filter and means for determining the second signal strength of the second signal output from the second filter.

19. The calibration circuit of claim 18 wherein the tuning means further comprises means for comparing the first signal suppression with the second signal suppression, the tuning means digitally tuning the first filter if the first signal suppression is lower than the second signal suppression and digitally tuning the second filter if the second signal suppression is lower than the first signal suppression.

20. The calibration circuit of claim 19 wherein the tuning means digitally tunes each of the first and second filters by providing a first digital word to the first filter and a second digital word to the second filter.

21. The calibration circuit of claim 15 wherein the first filter comprises a first resistor and a first tunable capacitor, and the second filter comprises a second resistor and second tunable capacitor, the tuning means digitally tuning the first and second capacitors.

22. The calibration circuit of claim 21 wherein the tuning means digitally tunes each of the first and second capacitors by providing a first digital word to the first capacitor and a second digital word to the second capacitor.

23. The calibration circuit of claim 22 wherein the tuning means comprises means for initially tuning the first capacitor to a first value and the second capacitor to a second value different from the first value, and means for latching a calibration digital word when the first digital word equals the second digital word, the calibration word being equal to the first and second digital word.

24. The calibration circuit of claim 23 wherein the first value comprises a maximum value of the first capacitor and the second value comprises a minimum value of the second capacitor.

25. The calibration circuit of claim 21 wherein the first capacitor comprises a first tunable capacitor array and the second capacitor comprises a second tunable capacitor array.

26. The calibration circuit of claim 25 wherein the first and second tunable capacitor arrays each comprises a plurality of capacitors coupled in parallel, and a plurality of switches each being coupled in series to a different one of their its respective capacitors.

27. The calibration circuit of claim 26 wherein the tuning means tunes the first filter with a plurality of first digital bits and tunes the second filter with a plurality of second digital bits, the first digital bits each controlling a different one of the switches in the first capacitor array and the second digital bits each controlling a different one of the switches in the second capacitor array.

28. A transceiver, comprising:

a calibration circuit having first and second digitally tunable filters, and control logic having a tuning output to digitally tune the first and second filters as a function of a first parameter of a first signal output from the first filter and a second parameter of a second signal output from the second filter; and

a digitally tunable transceiver filter tuned by the tuning output of the control logic.

29 The transceiver of claim 28 wherein the first and second filters each comprises a polyphase filter.

30. The transceiver of claim 28 wherein the first and second filters each comprises a notch filter.

31. The transceiver of claim 28 further comprising a first signal strength indicator to determine the first parameter and a second signal strength indicator to determine the second parameter.

32. The transceiver of claim 31 wherein the first parameter comprises a first signal suppression and the second parameter comprises a second signal suppression.

33. The transceiver of claim 32 further comprising a comparator to compare the first signal suppression to the second signal suppression, the control logic digitally tuning the first filter if the first signal suppression is lower than the second signal suppression and digitally tuning the second filter if the second signal suppression is lower than the first signal suppression.

34. The transceiver of claim 33 wherein the control logic digitally tunes each of the first and second filters by providing a first digital word to the first filter and a second digital word to the second filter.

35. The transceiver of claim 28 wherein the first filter comprises a first resistor and a first tunable capacitor, and the second filter comprises a second resistor and a second tunable capacitor, the control logic digitally tuning the first and second capacitors.

36. The transceiver of claim 35 wherein the first capacitor comprises a first tunable capacitor array and the second capacitor comprises a second tunable capacitor array.

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37. The transceiver of claim 36 wherein the first and second tunable capacitor arrays each comprises a plurality of capacitors coupled in parallel, and a plurality of switches each being coupled in series to a different one of their its respective capacitors.

38. The transceiver of claim 37 wherein the control logic tunes the first filter with a plurality of first digital bits and tunes the second filter with a plurality of second digital bits, the first digital bits each controlling a different one of the switches in the first capacitor array and the second digital bits each controlling a different one of the switches in the second capacitor array.

39. The transceiver of claim 35 wherein the control logic digitally tunes each of the first and second capacitors by providing a first digital word to the first capacitor and a second digital word to the second capacitor.

40. The transceiver of claim 38 wherein the control logic tunes initially tunes the first capacitor to a first value and tunes the second capacitor to a second value different from the first value, and wherein the control logic is disabled when the first digital word equals the second digital word.

41. The transceiver of claim 40 wherein the first value comprises a maximum value of the first capacitor and the second value comprises a minimum value of the second capacitor.

42. The transceiver of claim 40 wherein the control logic tunes the transceiver component calibration digital word, the calibration digital word being equal to the first and second digital word.

43. The transceiver of claim 42 wherein the transceiver filter comprises a transceiver resistor and a tunable transceiver capacitor.

44. The transceiver of claim 43 wherein the transceiver capacitor comprises a tunable capacitor array.

45. The transceiver of claim 44 wherein the tunable capacitor array comprises a plurality of capacitors coupled in parallel, and a plurality of switches each being coupled in series to a different one of the capacitors.

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46. The transceiver of claim 45 wherein the calibration digital word comprises a plurality of digital bits each controlling a different one of the switches.

47. A calibration circuit, comprising:

first and second digitally tunable filters each having a tuning input;

a first signal strength indicator having an input coupled to the first filter, and an output;

a second signal strength indicator having an input coupled to the second filter, and an output;

a comparator having an input coupled to the output of the first and second signal strength indicators, and an output; and

control logic having an input coupled to the output of the comparator, and a first tuning output coupled to the tuning input of the first filter and a second tuning output coupled to the tuning input of the second filter.

48. The calibration circuit of claim 47 wherein the first and second filters each comprises a polyphase filter.

49. The calibration circuit of claim 47 wherein the first and second filters each comprises a notch filter.

50. The calibration circuit of claim 47 wherein the first filter comprises a first resistor and a first tunable capacitor, and the second filter comprises a second resistor and a second tunable capacitor, the control logic digitally tuning the first and second capacitors.

51. The calibration circuit of claim 50 wherein the first capacitor comprises a first tunable capacitor array and the second capacitor comprises a second tunable capacitor array.

52. The calibration circuit of claim 51 wherein the first and second tunable capacitor arrays each comprises a plurality of capacitors coupled in parallel, and a plurality of switches each being coupled in series to a different one of their its respective capacitors.

53. The calibration circuit of claim 52 wherein the first tuning output comprises a plurality of first digital bits and and the second tuning output comprises a plurality of second digital bits, the first digital bits each controlling a different one of the switches in the first capacitor array and the second digital bits each controlling a different one of the switches in the second capacitor array.

54. A method of calibration, comprising:

providing a reference signal to first and second digitally tunable filters; and

digitally tuning the first and second filters as a function of a first parameter of the filtered reference signal output from the first filter and a second parameter of the filtered reference signal output from the second filter.

55. The method of claim 54 wherein the first and second filters each comprises a polyphase filter.

56. The method of claim 54 wherein the first and second filters each comprises a notch filter.

57. The method of claim 54 wherein the first parameter comprises a first signal suppression and the second parameter comprises a second signal suppression.

58. The method of claim 57 further comprising comparing the first signal suppression to the second signal suppression, wherein tuning of the first and second filters comprises digitally tuning the first filter if the first signal suppression is lower than the second signal suppression and digitally tuning the second filter if the second signal suppression is lower than the first signal suppression.

59. The method of claim 58 wherein the tuning of the first and second filters further comprises providing a first digital word to the first filter and a second digital word to the second filter.

60. The method of claim 54 wherein the first filter comprises a first resistor and first tunable capacitor, and the second filter comprises a second resistor and a second tunable capacitor, the tuning of the first and second filters comprising digitally tuning the first and second capacitors.

61. The method of claim 60 wherein the first parameter comprises a first signal suppression and the second parameter comprises a second signal suppression.

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62. The method of claim 61 wherein tuning of the first and second capacitors comprises initially tuning the first capacitor to a first value and the second capacitor to a second value different from the first value, the method further comprising comparing the first signal suppression to the second signal suppression with the first and second capacitors initially tuned, and wherein the tuning of the first capacitor further comprises digitally tuning the first capacitor if the first signal suppression is lower than the second signal suppression and digitally tuning the second filter if the second signal suppression is lower than the first signal suppression.

63. The method of claim 62 wherein the first value comprises a maximum value of the first capacitor and the second value comprises a minimum value of the second capacitor.

64. The method of claim 61 wherein tuning of the first and second capacitors comprises initially tuning the first capacitor to a first value and the second capacitor to a second value different from the first value, the method further comprising comparing the first signal suppression to the second signal suppression with the first and second capacitors initially tuned, and wherein the tuning of the first and second capacitors further comprises digitally tuning the first capacitor if the first signal suppression is lower than the second signal suppression.

65. The method of claim 64 wherein the tuning of the first and second capacitors further comprises providing a first digital word to the first capacitor and a second digital word to the second capacitor.

66. The method of claim 65 wherein the tuning of the first and second capacitors further comprises digitally tuning the first capacitor until the first signal suppression exceeds the second

signal suppression, comparing the first digital word to the second digital word, and digitally tuning the second capacitor if the first and second digital words are not equal.

67. The method of claim 65 wherein the tuning of the first and second capacitors further comprises digitally tuning the first capacitor until the first signal suppression exceeds the second signal suppression, comparing the first digital word to the second digital word, and latching a calibration digital word if the first and second digital words are equal, the calibration digital word being equal to the first and second digital word.

68. The method of claim 67 further comprising digitally tuning a transceiver filter with the calibration digital word.